Claims

We claim:

1. A transmission system, comprising:

a plurality of transmitters, each of the plurality of transmitters transmitting data in one of a plurality of transmission bands, at least one of the plurality of transmitters comprising

a trellis encoder coupled to receive data to be transmitted;

a symbol mapper coupled to receive output signals from the trellis encoder;

at least one digital to analog converter coupled to receive output signals from the symbol mapper;

at least one filter coupled to receive analog output signals from the at least one digital to analog converter; and

an up-converter coupled to receive output signals from the at least one filter and shift a frequency of the output signal to an assigned frequency.

2. The transmitter of Claim 1, wherein the symbol mapper is a 128 QAM symbol mapper.

3. The transmitter of Claim 1, wherein the encoder encodes the most-significant-bit of the data.

4. The transmitter of Claim 1, wherein the at least one filter is a low-pass filter with a cut off frequency and an excess bandwidth that passes a base-band data signal but substantially filters out higher frequency signals.

5. The transmitter of Claim 4, wherein the low-pass filter is a two-zero, five-pole filter with filter parameters chosen such that an output response of the at least one of the plurality of filters approximates a root raised cosine function.

6. The transmitter of Claim 5, wherein the filter parameters of the low-pass filter can be determined by minimizing a cost function of the low pass filter response convoluted with the digital-to-analog converter response and compared with a root raised cosine function.

7. A transmission system, comprising:

a plurality of receivers, each of the plurality of receivers receiving signals from one of a plurality of transmission bands, at least one of the plurality of receivers comprising:

a down converter that converts an input signal from the one of the plurality of transmission bands to a base band;

a filter coupled to receive signals from the down converter, the filter substantially filtering out signals not in the base band;

an analog-to-digital converter coupled to receive signals from the filter and generate digitized signals;

an equalizer coupled to receive the digitized signals; and

a trellis decoder coupled to receive signals from the equalizer and generate recreated data, the recreated data being substantially the same data transmitted by a corresponding transmitter.

8. The system of Claim 7, wherein the down-converter creates an in-phase signal and a quadrature signal, the in-phase signal being the input signal multiplied by a cosine function at the frequency of the one of the plurality of transmission bands and the quadrature signal being the input signal multiplied by a sine function at the frequency of the one of the plurality of transmission bands.

9. The system of Claim 8, wherein the filter includes an in-phase filter filtering the in-phase signal and a quadrature filter filtering the quadrature signal.

10. The system of Claim 9, further including an offset block coupled between the down-converter and the filter, the offset block offsetting the in-phase signal and the quadrature signal such that signals output from the analog-to-digital converter averages zero.

11. The system of Claim 8, further including an amplifier coupled between the filter and the analog-to-digital converter, the amplifier amplifying an in-phase filtered signal from the in-phase filter and a quadrature filter signal from the quadrature filter such that the analog-to-digital converter is filled.

12. The system of Claim 11, wherein an in-phase gain of the amplifier and the quadrature gain of the amplifier are adaptively chosen in an automatic gain controller.

13. The system of Claim 12, wherein the automatic gain controller sets the in-phase gain and the quadrature gain based on the digitized signals from the analog to digital converters.

14. The system of Claim 13, wherein the in-phase gain and the quadrature gain are equal.

15. The system of Claim 8, wherein the analog-to-digital converter includes a first analog-to-digital converter coupled to receive signals from the in-phase filter and a second analog-to-digital converter coupled to receive signals from the quadrature filter.

16. The system of Claim 15, further including a correction circuit coupled between the analog-to-digital converter and the equalizer.

17. The system of Claim 16, wherein the correction circuit includes an adjustment to correct phases between the in-phase signal and the quadrature signal.

18. The system of Claim 17, wherein a small portion of one of the in-phase signal and the quadrature signal are added to the opposite one of the in-phase signal and the quadrature signal.

19. The system of Claim 18, wherein a second portion of the opposite one of the in-phase signal and the quadrature signal is added to the opposite one of the in-phase signal and the quadrature signal.

20. The system of Claim 19, wherein the small portion and the second portion are adaptively chosen.

21. The system of Claim 20, wherein the small portion is a function of in-phase and quadrature output signals from the correction circuit.

22. The system of Claim 20, wherein the second portion is a function of the ratio between in-phase and quadrature signals from the correction circuit.

23. The system of Claim 8, wherein a phase rotator circuit is coupled between the analog-to-digital converter and the equalizer.

24. The system of Claim 23, wherein a parameter of the phase rotator circuit is adaptively chosen.

25. The system of Claim 8, wherein an amplifier is coupled between the equalizer and the trellis decoder.

26. The system of Claim 25, wherein a quadrature correction is coupled between the amplifier and the trellis decoder.

27. The system of Claim 26, wherein an offset circuit is coupled between the quadrature correction and the trellis decoder.

28. The system of Claim 25, wherein an in-phase gain and a quadrature gain of the amplifier are adaptively chosen from error signals calculated from sliced values.

29. The system of Claim 28, wherein the sliced values are determined from input signals to the trellis decoder.

30. The system of Claim 26, wherein a parameter of the quadrature correction is adaptively chosen.

31. The system of Claim 27, wherein a parameter of the offset circuit is adaptively chosen.

32. The system of Claim 7, wherein the equalizer is a complex equalizer executing a transfer function, the transfer function having parameters $C_k^x(j)$ and $C_k^y(j)$ where j is an integer.

33. The system of Claim 32, wherein the center parameters $C_k^x(0)$ and $C_k^y(0)$ are fixed.

34. The system of Claim 33, wherein $C_k^x(0)$ is one and $C_k^y(0)$ is zero.

35. The system of Claim 33, wherein the parameters $C_k^x(-1)$ and $C_k^y(-1)$ are fixed.

36. The system of Claim 35, wherein the parameter $C_k^x(-1)$ is about -0.3125.

37. The system of Claim 35, wherein the parameter $C_k^y(-1)$ is about -0.015625.